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(54) SEMICONDUCTOR DEVICE MANUFACTURE

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare

the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a method of manufacturing a semiconductor device comprising a semiconductor body having at least one insulated gate field effect transistor, and further relates to a semiconductor device manufactured using this method.

Various methods are known of manufacturing a semiconductor device comprising a semiconductor body having at least one insulated gate field effect transistor, in which in a first region of a first conductivity type adjoining a surface of the body a second region of the second conductivity type which also adjoins said surface is provided. The second region forms with the first region a *p-n* junction which intersects the said surface in a closed curve. The source and drain zones of a field effect transistor are provided in the second region.

These known methods are of importance, *inter alia*, because the structure obtained with said methods, in which the source and drain zones of the relevant field effect transistor are situated in a region which is surrounded by another region of the opposite conductivity type and is separated therefrom by a *p-n* junction, presents the possibility of realizing interesting and very advantageous semiconductor structures. Several semiconductor circuit elements may be provided in one and the same semiconductor body, separate circuit elements or groups of circuit elements being mutually separated electrically from each other within the semiconductor body. Very important are the possibility of providing field effect transistors of a complementary structure (*n-p-n* and *p-n-p*) in the same semiconductor body, and the possibility of manufacturing, simultaneously and without extra diffusion steps, one or more bipolar transistors in the same body beside the relevant field effect transistor or field effect transistors.

In a method as described above it is of very great importance that the said second region in which an insulated gate field effect transistor is provided has an accurately defined, comparatively low surface concentration of the doping material determining the conductivity type of the second region at least in the part of said region (the channel region) situated between the source and drain zones of said field effect transistor; said surface concentration should also be very readily reproducible. Actually, even with very small differences in said surface concentration, considerable differences occur in the threshold value of the voltage between the gate electrode and the channel region, which causes the relevant field effect transistor to change from the non-conducting into the conducting state.

When using known methods, it has proved particularly difficult in practice to realize in a reproducible manner the low surface concentrations which are required for the most desirable threshold voltages, for example, between −3 volts and +3 volts.

According to a first known method, the second region is provided by diffusion of a doping material of the second conductivity type from the semiconductor surface in the first region of the first conductivity type. However, when using said method it is extremely difficult to obtain the desirable very low surface concentration (10^{16}—10^{17} atoms/cc) for the doping of the second region in a reproducible manner. In this manner, higher surface concentrations (10^{18}—10^{20} atoms/cc) can be realized simply and in a reproducible manner, but these give rise to inadmissibly high threshold voltages of the field effect transistor.

According to a second known method, the second region is formed by providing locally on a substrate a highly doped layer of the second conductivity type after which a layer of the first conductivity type is grown epitaxially on the substrate and said highly doped layer. During said epitaxial growth or during a subsequent heating step, the highly doped layer diffuses in the substrate and in the epitaxial layer up to the surface. As a result of said diffusion, the conductivity type of the epitaxial layer is locally inverted above the buried layer as a result of which the second region of the second conductivity type is formed having a comparatively low doping concentration at the semiconductor surface. Not counting the fact that it is necessary to provide an epitaxial layer and a buried layer with a suitable doping material, an important drawback of this method is that the reproducibility of the resulting low surface concentration is *inter alia* highly dependent upon the reproducibility of the thickness of the epitaxial layer through which the diffusion from the buried layer takes place. A small difference in this thickness may result in an inadmissible deviation in the surface concentration and hence in the threshold voltage of the field effect transistor.

A common drawback of the two described known methods is furthermore that, when a sufficiently low surface doping of the second region is achieved, said concentration is so low that inversion channels can easily be formed at the surface, for example below an oxide layer, whether or not under the influence of an electric field induced by a metal layer situated on said oxide layer.

According to a third known method, a doping material of the second conductivity type is locally provided on the semiconductor surface of a region of the first conductivity type while using a first mask, after which a second mask having an aperture within the doped surface region is provided on the doped region and the doping material is then indiffused by heating in moist oxygen. During said diffusion an oxide layer is formed on the surface within the said aperture, in which layer a part of the doping material is incorporated. As a result of this a region of the second conductivity type is formed which is thicker at the edge and has a higher surface concentration than below the aperture. In the region of comparatively low surface concentration below the aperture, source and drain zones of a field effect transistor may then be provided.

In addition to the fact that the thickness of the region of the second conductivity type obtained by using the said last-mentioned method is inhomogeneous and that the use of two masks is indispensable, it is difficult to obtain the desirable low surface concentrations by diffusion in an oxidizing atmosphere in a reproducible manner.

According to the present invention there is provided a method of manufacturing a semiconductor device comprising a semiconductor body having at least one insulated gate field effect transistor, which body comprises a first region of a first conductivity type adjoining a surface of the body and a second region of the second conductivity type which also adjoins said surface, said second region forming with the first region a *p-n* junction which intersects the said surface in a closed curve, and source and drain zones of a field effect transistor being present in said second region, in which method, in order to form the second region, a doping material determining the second conductivity type is introduced in the first region from the semiconductor surface, after which said doping material is partially diffused out from the semiconductor body in a space having an atmosphere of reduced pressure over at least part of the semiconductor surface occupied by the second region, as a result of which a peak value of the concentration of the said doping material occurs in a zone of the second region situated between the first region and the semiconductor surface part from which the outdiffusion took place, and in order to form the source and drain zones, zones of the first conductivity type are provided at least partly in that part of the second region in which, as a result of the outdiffusion, the doping concentration increases from the semiconductor surface, which part of the second region is hereinafter termed the part having a positive doping gradient.

By using the method according to the invention, a second region of the second conductivity type is obtained which shows a readily-defined, reproducible, low surface concentration at least over a part of its surface as a result of which the threshold voltage of the field effect transistor or field effect transistors provided in said region is also very readily controllable and reproducible. Such a reproducible and comparatively low surface concentration which is hard to achieve according to known methods can be realized in a simple manner according to the invention by outdiffusion under reduced pressure, and if desired the same mask may be used when introducing and outdiffusing said doping material.

Said reduced pressure may be given various values while the atmosphere in which the outdiffusion takes place may have a variety of compositions. However, the best results are obtained when the outdiffusion is carried out in a vacuum. Furthermore, a quantity of semiconductor material is preferably provided in the space containing the atmosphere of reduced pressure (and

vacuum, respectively) which quantity is substantially free from the doping material to be outdiffused so as to prevent material of the semiconductor body from evaporating partly.

When the doping material is outdiffused over only a part of the surface of the second region, the part having a positive doping gradient will be bounded by a part of the second region having a higher surface concentration in which the doping concentration decreases continuously from the surface to the interior. The source and drain zones of the field effect transistor may be provided partly in said part having a higher surface concentration, on the understanding that the region between the source and drain zones belongs to the part having a low surface concentration and a positive doping gradient. Preferably, however, the source and drain zones of the first conductivity type are provided entirely in the said part having a positive doping gradient of the second region, said zones being surrounded entirely by said part within the body. As a result of this, the breakdown voltage between the source and drain zones and the second region is high, which is desirable in most of the cases.

In those cases in which the doping material is outdiffused only over a part of the semiconductor surface occupied by the second region, at least the edge of the surface portion occupied by the second region is preferably covered during the outdiffusion by a masking layer which impedes the outdiffusion of the doping material from the semiconductor surface. The edge of the second region covered by the masking layer thereby obtains a high doping concentration at the surface as a result of which the formation of inversion channels at the surface between the first and the second region is prevented or at least seriously impeded. The introduction and outdiffusion of the doping material of the second conductivity type may advantageously be carried out while using the same diffusion mask, as a result of which a minimum of masking steps is required.

In a further preferred form, the doping material is outdiffused over at least two mutually separated parts of the semiconductor surface occupied by the second region, and the source and drain zones of respective insulated gate field effect transistors are provided in each of the said parts. For example, several field effect transistors may be formed within the second region, which transistors are each surrounded by a surface part of the second region from which no outdiffusion has taken place and of which consequently the surface concentration is sufficiently high to avoid the formation of inversion channels between the field effect transistors.

In an important preferred form, a complementary insulated gate field effect transistor having source and drain zones of the second conductivity type adjoining the surface is provided in the first region of the first conductivity type beside the second region of the second conductivity type beside the second region of the second conductivity type. Thus, there can be provided in a very simple, efficacious and reproducible manner structures having complementary field effect transistors which may be used in many important circuit arrangements. In this preferred form the second region itself may furthermore constitute advantageously a source or drain zone of the complementary field effect transistor so that only one further electrode zone of said transistor need be provided in addition to the gate electrode.

These processes in accordance with the present invention can be combined in an advantageous manner with the manufacture of bipolar structures without extra indiffusion steps being necessary. Thus in a further preferred form a bipolar transistor of which the base zone is provided simultaneously with the second region and the emitter zone is provided simultaneously with the source and drain zones of the field effect transistor in the second region is provided in the first region beside the second region.

The second region may be surrounded partly by the first region and adjoin for the remaining part, for example, a substrate region of the second conductivity type. In an important preferred form, however, the second region is surrounded entirely by the first region within the semiconductor body so that the *p-n* junction between the first and the second region only intersects the semiconductor body at the said surface. The second region may then form, for example, in itself an island of an integrated monolithic circuit isolated by said *p-n* junction.

The first region may be an epitaxial layer of the first conductivity type provided on a substrate region of the second conductivity type, which layer is divided into islands by isolation zones of the second conductivity type extending from the surface to the substrate region, and said isolation zones and the second region may be provided simultaneously in the same diffusion step by indiffusion of a doping material determining the second conductivity type. This process for manufacturing a monolithic integrated circuit saves a diffusion step for providing the second region. Furthermore, standard diffusions, with comparatively high surface concentrations, which are conventional for the manufacture of the rest of the circuit may be used so that besides the said outdiffusion few or no extra processing steps are necessary.

Although the second region may be of the *n*-conductivity type in which for the

formation of said second region a donor is introduced, preferably a *p*-type conductive second region is formed by introduction of an acceptor. It has actually been found in practice, in particular when the semiconductor body consists of silicon, that in order to obtain an insulated gate *p-n-p* field effect transistor having the desired threshold voltage, a considerably lower surface concentration of the (*n*-type) channel region is required than in an *n-p-n* field effect transistor. This is related to the fact that when conventional masking and diffusion techniques are used, the electrostatic charge in the resulting oxide is positive so that a negative surface charge is induced in the underlying surface of the semiconductor body. This is the case in particular in the silicon silicon-oxide system.

When the semiconductor body consists of silicon, boron is preferably used as an acceptor impurity to form the second region. Boron has proved to be particularly suitable to obtain the desirable low surface concentration by using the outdiffusion process described. To obtain a field effect transistor having a threshold voltage of at most 3 volt which is in addition surrounded by a channel interrupting zone, the surface concentration of the boron during the introduction and the time and temperature of the outdiffusion are preferably chosen such that after the outdiffusion the maximum doping concentration in the second region is at least equal to 10^{18} atoms/cc and that the doping concentration at the surface part of the second region across which the outdiffusion took place is at most equal to 5×10^{16} atoms/cc.

A few embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a diagrammatic plan view of a device manufacturing by using a method in accordance with the invention;

Figure 2 is a diagrammatic cross-sectional view taken on the line II—II of the device shown in Figure 1;

Figures 3 to 8 are diagrammatic cross-sectional views taken on the line II—II of the device shown in Figures 1 and 2 in successive stages of manufacture;

Figure 9 shows the doping profile taken on the line IX—IX of Figures 5 and 6 prior to and after the outdiffusion, and

Figures 10 to 14 are diagrammatic cross-sectional views of other devices manufactured by using methods in accordance with the invention.

The drawings are diagrammatic and not to scale; this applies in particular to the dimensions in the direction of thickness and to the thicknesses of the insulating layers. Corresponding components in the Figures are referred to by the same reference numerals as much as possible.

The device of Figures 1 and 2 comprises a semiconductor body 1 of silicon consisting of a *p*-type substrate region 2 on which an epitaxial *n*-type layer is grown which constitutes a first region 3 adjoining a surface 4 of the body. A second *p*-type conductive region 6 which also adjoins the surface 4 constitutes with the first region 3 a *p-n* junction 5 which intersects the surface 4 in a closed curve 7 (see Figure 1).

N-type source and drain zones 8 and 9 of an (*n-p-n*) insulated gate field effect transistor 12 are provided in the second region 6. The *p*-type region 6 has a doping concentration which is maximum in a zone on and near the contour 10 which is shown in broken lines in the Figures. The doping concentration in the part 11 of the second region 6 between the contour of maximum doping concentration 10 and the semiconductor surface 4 increases inwards from the surface 4; this part 11 is therefore termed the part having a positive doping gradient. The source zone 8 and the drain zone 9 are both situated entirely in the part 11 of the region 6 and are entirely surrounded within the body by said part 11.

A complementary (*p-n-p*) field effect transistor having an insulated gate electrode 13 and *p*-type source and drain zones 14 and 15 is provided in the first region 3 beside the second region 6. Furthermore a bipolar transistor having a *p*-type base zone 16 and an *n*-type emitter zone 17 is provided in an island-shaped part of the region 3 which is separated by in-diffused *p*-type isolation zones 18 from the remaining part of the region 3 and constitutes the collector zone of the bipolar transistor. Said collector zone comprises a highly doped *n*-type buried layer 19 and a highly doped *n*-type contact zone 20 to reduce the collector resistance.

The semiconductor surface 4 is covered with a silicon oxide layer 21 and the zones 8, 9, 14, 15, 16, 17 and 20 are contacted *via* windows in the oxide layer 21 by means of aluminium layers 22, 23, 24, 25, 26, 27 and 28. The gate electrodes 12 and 13 are also constituted by aluminium layers. The two field effect transistors and the bipolar transistor together form part of a monolithic integrated semiconductor circuit.

In accordance with the present invention the device described is manufacured in the following manner (see Figures 3 to 8). Starting material (see Figure 3) is a *p*-type silicon substrate 2, resistivity 5 ohm.cm, thickness 200 microns. Afer having made a (111) surface of said substrate free from crystal defects as much as possible by polishing and etching, said surface is thermally oxidized. An aperture is then etched in the resulting oxide layer and arsenic is diffused in said

aperture to form an n-type layer 19 having a sheet resistance of 20 ohm per square, see Figure 3. The oxide is then removed and an *n*-type silicon layer 3 having a thickness of 5 microns and a resistivity of 3 ohm.cm is grown on the substrate 2 by using conventional epitaxial growth method. During said growth the layer 19 partly diffuses in the substrate 2 and partly in the layer 3, see Figure 4.

An oxide layer 30, 0.9 micron thick, is obtained on the surface 4 of the layer 3 by thermal oxidation. Apertures are etched in said oxide layer 30 by means of known photolithographic etching methods. Boron is diffused in said apertures, *p*-type zones 18 and 6 being formed, see Figure 5. The surface concentration of said boron diffusion gives a sheet resistance of 150 ohm per square. During said diffusion a layer of borosilicate glass is formed within the apertures.

By a superficial etching treatment the oxide glass layer 30 is etched away through part of its thickness over the whole surface until the semiconductor surface within the diffusion windows through which the zones 6 and 18 were indiffused, is exposed. The remaining oxide has a thickness of approximately 0.4 micron.

The silicon plate is now placed in a quartz glass ampoule in which pure undoped silicon powder is provided. The ampoule is evacuated and sealed. For outdiffusion, the ampoule is then heated in a furnace at a temperature of 1200°C for 4 hours. Boron diffuses out of the surface to the exterior from the parts of the diffused regions not covered by oxide. The outdiffused boron is taken up partly in the silicon powder and partly in the wall of the quartz ampoule. As a result of the presence of the silicon powder, a certain silicon vapour pressure prevails in the ampoule which counteracts the evaporation of silicon at the surface. The outdiffusion of boron from the region 6 occurs in this case via the same aperture in the oxide layer through which the boron was first indiffused so that no extra mask is necessary for this outdiffusion. During the outdiffusion, the edge of the surface occupied by the region 6, which edge is formed during the indiffusion by the lateral diffusion below the edge of the diffusion mask, is covered with an oxide layer masking against the outdiffusion.

The condition after the outdiffusion is shown in Figure 6. The zones 6 and 18 extend throughout the thickness of the epitaxial layer 3, the zones 18 constituting isolation zones which divide the layer 3 into islands. By the outdiffusion of boron, a narrow zone (10) of maximum boron concentration has been formed in the region 6 between the exposed part of the surface 4 and the region 3 on and in the immediate proximity of the contour 10 which is denoted in the Figures by broken lines and which extends up to the surface 4. The boron concentration decreases from the zone 10 towards both sides and the part 11 of the region 6 has a doping concentration which increases from the surface inwardly, in other words it has a positive doping gradient.

After the outdiffusion, the boron concentration at the surface of the region 6 within the window through which the outdiffusion took place is approximately 5.10^{16} atoms/cc and below the layer, where substantially no outdiffusion took place, approximately 2.10^{18} atoms/cc. This latter doping concentration is sufficient to prevent an inversion layer from being formed at the area in the region 6 below the oxide layer. Figure 9 shows diagrammatically the variation of the boron concentration C with the depth *x* below the surface 4 taken on the line 1X—1X of Figures 5 and 6, curve A being the profile prior to the outdiffusion and curve B being the profile after the outdiffusion. The zone of maximum boron concentration is approximately 1.4 microns below the semiconductor surface.

A thermal oxidation is then performed to close the apertures in the oxide layer by forming an oxide layer, 0.3 micron thick. After etching new diffusion windows the base zone 16 and the source and drain zones 14 and 15 are simultaneously formed by a boron diffusion with a surface concentration of 5.10^{18} atoms/cc and a depth of penetration of 1.5 microns (sheet resistance 200 ohm per square), see Figure 7. The emitter zone 17, the collector contact zone 20 and the source and drain zones 8 and 9, see Figure 8, are then provided by a phosphorus diffusion (sheet resistance 5—6 ohm per square, depth of penetration 1 micron). These latter zones 8 and 9 lie entirely in the part 11 having a positive doping gradient and are fully surrounded by said part.

Finally the oxide is removed at the area of the gate electrodes to be provided and is replaced by a new layer of thermally grown oxide, 0.1 micron thick (oxidation at 1000° C in moist oxygen for 30 minutes). After etching contact windows the aluminium layers 12, 13 and 22 to 28 are then provided by using conventional vapour deposition and masking methods.

Since the source and drain zones 8 and 9 adjoin only comparatively low-doped p-type material, the breakdown voltage between said zones and the region 6 is high (approximately 20 volts). As a result of the comparatively high surface concentration of the zone 10, shortcircuit between the zones 8 and 9 and the region 3 *via* inversion channels is avoided. According to the method described, the bipolar transistor (17, 16, 3) and the complementary field effect transistors (8, 9, 12) and (14, 15, 13) can be manufac-

tured simultaneously while using normal standard diffusion using as an extra step only an outdiffusion. The field effect transistor (8, 9, 12) has threshold voltage of $+1\frac{1}{2}$ volt and the field effect transistor (14, 15, 13) has threshold voltage of $-1\frac{1}{2}$ volt (gate electrode voltage relative to the channel region).

A few other semiconductor devices which can be manufactured in accordance with the invention are shown in Figures 10 to 14. In these Figures, the components which correspond to components of the device of the previously described embodiment are referred to by the same reference numerals.

Figure 10 shows a structure having two complementary insulated gate field effect transistors of which the *n*-type source and drain electrodes 8 and 9 of the *n*-*p*-*n* field effect transistor are provided in the outdiffused part 11 having a positive doping gradient of the *p*-type second region 6 and in which said region 6 is diffused in the *n*-type first region 3 and is entirely surrounded by said region 3 without the use of an epitaxial layer. In addition to the *n*-*p*-*n* transistor (8, 9, 12) a complementary field effect transistor (14, 15, 13) is provided in the region 3 and is isolated from the field effect transistor (8, 9, 12) by the *p*-*n* junction 31 between the regions 3 and 6, while the zone 10 of maximum doping concentration extending up to the surface serves as a channel stopper and prevents the formation of an *n*-type inversion channel between the region 3 and the source and drain zones 8 and 9.

Figure 11 shows a variation of the structure of Figure 10 in which the source and drain zones of the complementary field effect transistor are constituted by the region 6 and a further *p*-zone 40 which, if desirable, may be provided simultaneously with the region 6 in the same diffusion step. The gate electrode 41 of the complementary transistor is provided between the zones 6 and 40 on the insulating layer.

Figures 12 and 13 illustrate the manufacture of a device in which several field effect transistors are provided in the region 6. As shown in Figure 12, several windows 50 are etched, after the indiffusion of the region 6 in the oxide layer on the surface by an extra masking and etching step, after which the outdiffusion takes place *via* said windows. Source and drain zones (8, 9) are then provided (see Figure 13) in each of the resulting regions 11 having a positive doping gradient so as to form several field effect transistors in the same region 6 which are each surrounded by a channel stopper zone having a comparatively high surface concentration which prevents shortcircuit *via* an inversion layer between source and drain zones of various transistors.

Figure 14 shows a device in which beside the second region 6 in the first region 3 a zone 60 of the same conductivity type as the region 6 is provided, which zone 60 constitutes the base zone of a bipolar transistor having an emitter zone 61 and a collector contact zone 62. The zone 60 is advantageously provided simultaneously with the region 6, and the zones 61 and 62 are advantageously provided simultaneously with the source and drain zones 8 and 9.

All the devices described may be manufactured while using the same processes which were described in the embodiment shown in Figures 1 to 9. For the manufacture of a device of the type of Figures 12 and 13 an extra masking and etching step is necessary.

Although in the description of the abovementioned embodiments the starting material was a structure in which the region 6 is of *p*-type conductivity, the conductivity types may of course be replaced, if desirable, by their opposite conductivity types while using the same methods. The outdiffusion may furthermore be carried out in an atmosphere of low pressure rather than a vacuum. Furthermore, if this should be desirable, for example, from a point of view of space saving, the source and drain zones 8 and 9 may be partly provided in parts of the region 6 outside the parts having a positive doping gradient, although as a result of this the breakdown voltage between the source and drain zones (8, 9) and the region 6 decreases. The whole surface of the region 6 may also be exposed prior to the outdiffusion as a result of which the outdiffusion takes place throughout said surface.

Many variations are possible to those skilled in the art without departing from the scope of this invention. Semiconductor materials other than silicon may be used, for example germanium and III-V compounds, for example gallium arsenide; other insulating layers than silicon oxide may be used, for example, silicon nitride, aluminium oxide or composite layers of two or more different materials on each other, and other metal layers may be used. The gate electrodes of some or of all the field effect transistors may also advantageously consist of other materials, in particular, polycrystalline silicon, instead of metal. Furthermore, other geometric structures may be used and in addition to insulated gate field effect transistors and bipolar transistors, other semiconductor circuit elements may be provided in the semiconductor body. Moreover the introduction of the doping material determining the second conductivity type prior to the outdiffusion may be carried out by other methods than indiffusion, for instance by ion implantation.

WHAT WE CLAIM IS:—

1. A method of manufacturing a semi-

conductor device comprising a semiconductor body having at least one insulated gate field effect transistor, which body comprises a first region of a first conductivity type adjoining a surface of the body and a second region of the second conductivity type which also adjoins said surface, said second region forming with the first region a *p-n* junction which intersects the said surface in a closed curve, and source and drain zones of a field effect transistor being present in said second region, in which method, in order to form the second region, a doping material determining the second conductivity type is introduced in the first region from the semiconductor surface, after which said doping material is partially diffused out from the semiconductor body in a space having an atmosphere of reduced pressure over at least part of the semiconductor surface occupied by the second region, as a result of which a peak value of the concentration of the said doping material occurs in a zone of the second region situated between the first region and the semiconductor surface part from which the outdiffusion took place, and in order to form the source and drain zones, zones of the first conductivity type are provided at least partly in that part of the second region in which, as a result of the outdiffusion, the doping concentration increases from the semiconductor surface, which part of the second region is hereinafter termed the part having a positive doping gradient.

2. A method as claimed in Claim 1, in which the doping material is outdiffused in a vacuum.

3. A method as claimed in claim 1 or Claim 2, in which a quantity of semiconductor material which is substantially free from the doping material to be outdiffused is provided in the space having the atmosphere of reduced pressure.

4. A method as claimed in any of the preceding Claims, in which the source and drain zones of the first conductivity type are provided entirely in that part of the second region having a positive doping gradient, said zones being surrounded within the body entirely by that part of the second region.

5. A method as claimed in any of the preceding Claims, in which the doping material which is introduced to form the second region is outdiffused only over a part of the semiconductor surface occupied by the second region, at least the edge of the surface portion occupied by the second region being covered during the outdiffusion by a masking layer which impedes the outdiffusion of the doping material from the semiconductor surface.

6. A method as claimed in Claim 5, in which the introduction and the outdiffusion of the doping material of the second conductivity type are carried out while using the same diffusion mask.

7. A method as claimed in Claim 5, in which the doping material is outdiffused over at least two mutually separated parts of the semiconductor surface occupied by the second region, and the source and drain zones of respective insulated gate field effect transistors are provided in each of the said parts.

8. A method as claimed in any of the preceding Claims, in which a complementary insulated gate field effect transistor having source and drain zones of the second conductivity type adjoining the semiconductor surface is provided in the first region of the first conductivity type beside said second region of the second conductivity type.

9. A method as claimed in Claim 8, in which the second region constitutes a source or drain zone of the complementary field effect transistor.

10. A method as claimed in any of the preceding Claims, in which a bipolar transistor of which the base zone is provided simultaneously with the second region and the emitter zone is provided simultaneously with the source and drain zones of the field effect transistor in the second region is provided in the first region beside the second region.

11. A method as claimed in any of the preceding Claims, in which the second region is surrounded entirely by the first region within the semiconductor body.

12. A method as claimed in any of Claims 1 to 10, in which the first region is an epitaxial layer of the first conductivity type provided on a substrate region of the second conductivity type, which layer is divided into islands by isolation zones of the second conductivity type extending from the surface to the substrate region, and said isolation zones and the second region are provided simultaneously in the same diffusion step by indiffusion of a doping material determining the second conductivity type.

13. A method as claimed in any of the preceding Claims, in which in order to form the second region an acceptor impurity is introduced.

14. A method as claimed in Claim 13, in which the semiconductor body consists of silicon, and boron is used as the acceptor impurity.

15. A method as claimed in Claim 14, in which the surface concentration of the boron during the introduction and the time and temperature of the outdiffusion are chosen such that after the outdiffusion the maximum doping concentration in the second region is at least equal to 10^{18} atoms/cc and that the doping concentration at the surface part of the second region across which the

outdiffusion took place is at most equal to 5×10^{16} atoms/cc.

16. A method as claimed in any of the preceding Claims, in which at least one field effect transistor has an insulated gate electrode of polycrystalline silicon.

17. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 1 to 9 of the accompanying drawings.

18. A method of manufacturing a semiconductor device, substantially as described with reference to Figures 11 and 12 of the accompanying drawings.

19. A semiconductor device manufactured by using a method as claimed in any of the preceding Claims.

20. A semiconductor device substantially as herein described with reference to Figure 10 of the accompanying drawings.

21. A semiconductor device substantially as herein described with reference to Figure 11 of the accompanying drawings.

22. A semiconductor device substantially as herein described with reference to Figure 14 of the accompanying drawings.

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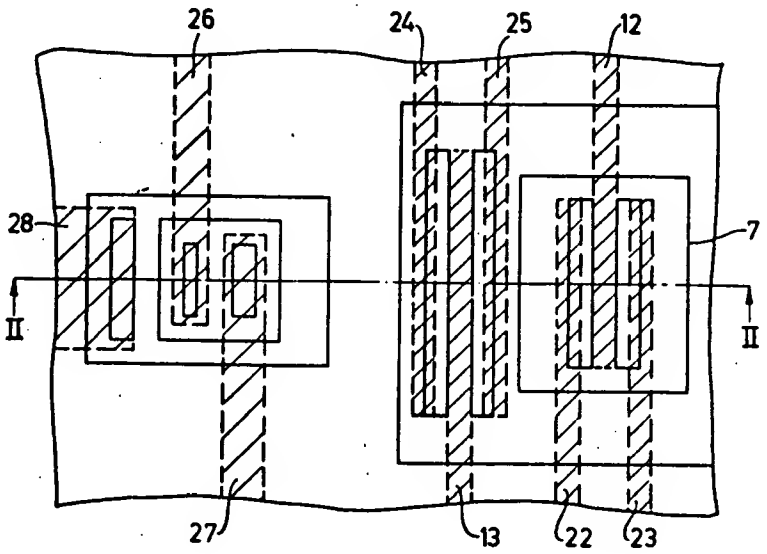
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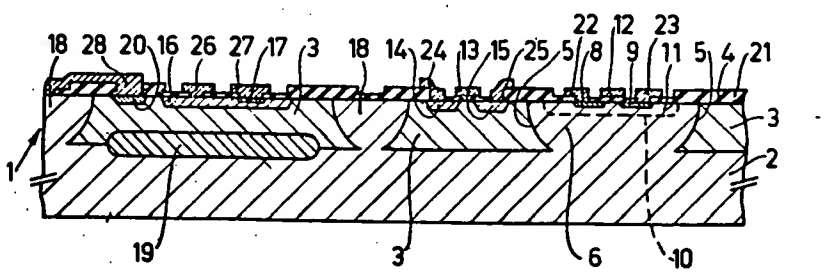
Fig.1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10

Fig.2

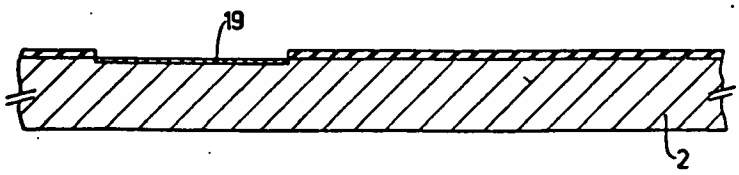

Fig.3

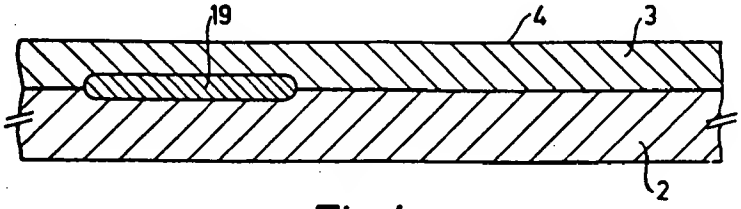

Fig.4

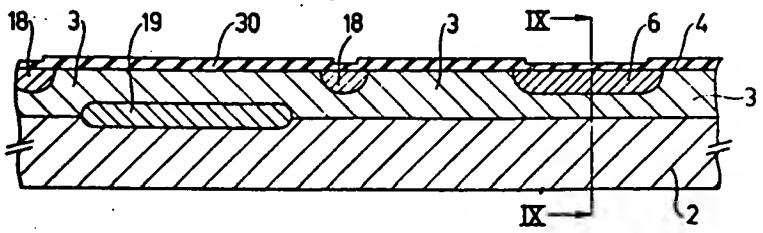

Fig.5

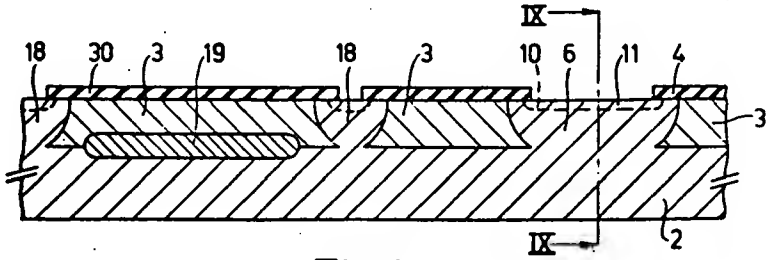

Fig.6

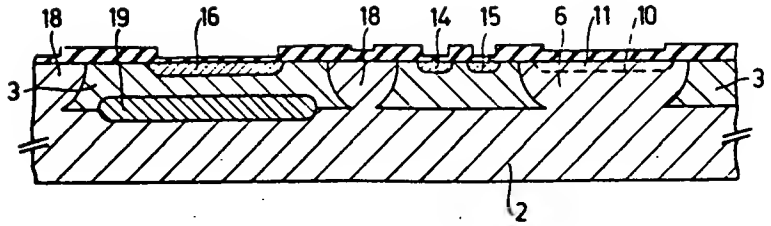

Fig.7

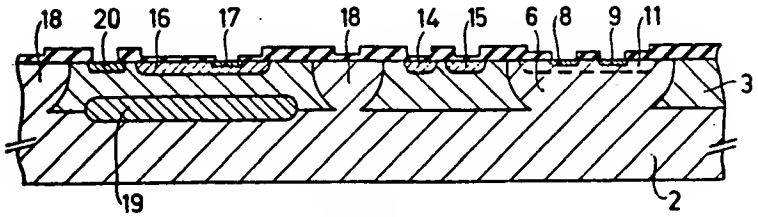

Fig.8

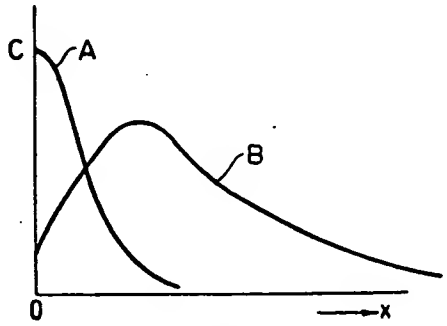

Fig.9

1372086 COMPLETE SPECIFICATION
4 SHEETS

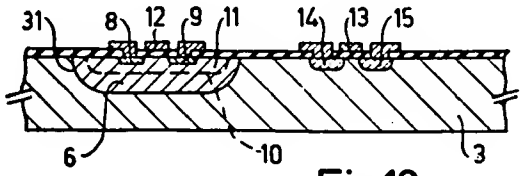

Fig.10

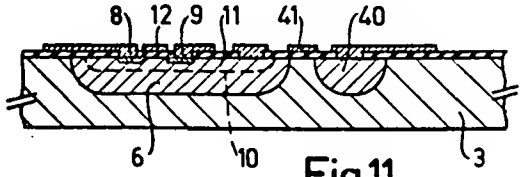

Fig.11

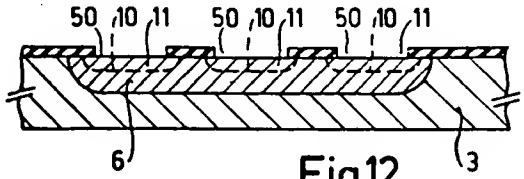

Fig.12

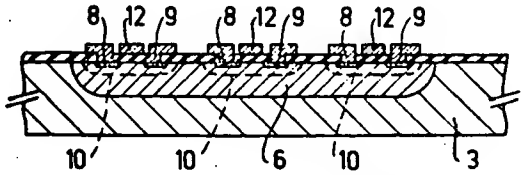

Fig.13

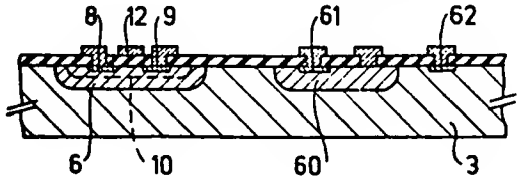

Fig.14